A VLSI Single Chip (255, 223) Reed-Solomon Encoder

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This article presents a description of a working single chip implementation of a Reed-Solomon encoder. The code used is the CCSDS (Consultative Committee on Space Data Systems) standard (255, 223) code. The architecture that leads to this single VLSI chip design makes use of a bit-serial finite field multiplication algorithm of E. R. Berlekamp.

I. Introduction

A concatenated coding system consisting of a convolutional inner code and a Reed-Solomon outer code has been adopted as a guideline for downlink telemetry for future space missions by CCSDS (Consultative Committe for Space Data Systems) (Ref. 1). The participants in this committee include the European Space Agency (ESA) and NASA as well as space agencies from many other nations. The convolutional inner code is the same (7, 1/2) code used by NASA's Voyager project. The outer Reed-Solomon code is a (255, 223) block code on 8-bit symbols and it is capable of correcting up to 16 symbol errors. The performance of such schemes is investigated in Ref. 2 where it is shown that this concatenated channel provides a coding gain of almost 2 dB over the convolutional-only channel at a decoded bit error rate of 10^{-5}. One of the benefits of concatenated coding, and one of the main motivations for its acceptance as a standard system, is that it provides for a nearly error-free communications link at fairly low signal power levels. This means that source data compression techniques (Ref. 3) can be used to help increase channel throughput without a substantial change in overall error rate. An end-to-end study of a system using concatenated coding with data compression can be found in Ref. 4.

A Reed-Solomon encoder is basically a circuit which performs polynomial division in a finite field. Such circuits are well known (Ref. 5) and their implementation is straightforward. The major problem in designing a small encoder is the large quantity of hardware that is necessary to perform the finite field multiplications. Due to the limited weight, space and power that can be allotted to a spacecraft instrument, the equipment used must be as light and as small as possible. Therefore, a single chip Reed-Solomon encoder can be a significant advantage in deep-space probe missions. This encoder represents a considerable space, weight and power savings over the smallest existing encoder (about 30 chips).

A conventional encoder described in Ref. 5 for the (255, 223) RS code, requires 32 finite field multipliers. These multipliers are usually implemented as full parallel multipliers or table look-up multipliers. The use of either of these multiplication algorithms prohibits the implementation of the encoder on a single medium density VLSI chip.

Fortunately, E. R. Berlekamp (Ref. 6) developed a serial algorithm for finite field multiplication. Berlekamp's algorithm requires only shifting and exclusive-or operations. Recently, it

was shown (Ref. 7) that this multiplication algorithm has enabled the design of a workable VLSI architecture, and that this new dual-basis (255, 223) RS encoder can be realized readily on a single VLSI chip with NMOS technology. This article presents the results of the implementation and testing of the RS encoder.

II. A Single VLSI Chip of a (255, 223) RS Encoder

Berlekamp's bit-serial multiplication algorithm for a (255, 223) RS-encoder over GF(2^8) is presented in Refs. 6 and 7.[1] A VLSI architecture for implementing this encoder using Berlekamp's multiplication algorithm is presented in Ref. 7. The block diagram of the (255, 223) RS encoder is exhibited here in Fig. 1.[2] In Fig. 1, one observes that the circuit is divided into five units: the Product unit, Remainder unit, Quotient unit, I/O unit, and Control unit. The use of each unit is explained in detail in Ref. 7. An overall block diagram of the implemented chip is shown in Fig. 2. In Fig. 2, VDD and GND are power pins. The signals ϕ_1 and ϕ_2 are the two phases of a system clock. The information symbols are fed into the chip serially through the data-in pin, DIN. Similarly, the encoded codeword is transmitted out of the chip sequentially from the date-out pin, DOUT. The control signal SL is set to 1 (logic 1) when the information symbols are loaded into the chip. After this, SL is set to 0. The control signal "START" resets a 3-bit word counter in this chip before the encoding process begins.

The entire chip was simulated on a general purpose computer using ESIM (a logic-level simulation program; see Ref. 8) and SPICE (a transistor level circuit simulation program; see Ref. 9). The layout of the encoder was accomplished using the program CAESAR (Ref. 10). LYRA (Ref. 11) was used to check the resulting layout against a set of geometric rules supplied by the fabricator. Timing simulation was done using CRYSTAL (Ref. 13). The circuit comprises about 3000 transistors. It was fabricated using the MOSIS service (Ref. 12) and the technology used was 4 μm NMOS. The layout of the encoder[3] was modified and the new version is shown in Fig. 3(a). A photograph of a fabricated chip is shown in Fig. 3(b).

III. The Procedure for Testing a (255, 223) RS Encoder

The testing of this chip was accomplished at the Jet Propulsion Laboratory (JPL). The JPL testing system consists of a custom-built general purpose hardware tester called the Digital Microcircuit Functionality Tester (DMFT) (Ref. 14) and a VAX 11/750 computer. A program called "Logic" (Ref. 14) acts as an interface between these two subsystems. Logic is a program which allows a chip designer to create a set of test vectors for the functional simulation and testing of a circuit. Two types of tests are supported currently. The first is a link to the ESIM logic simulator. The second is an interface to the DMFT tester. Logic can read and edit files that contain test vector and tester configuration information. Once a set of test vectors is generated, they may be saved or applied to either ESIM or the DMFT tester. The results are displayed on the terminal screen in a logic analyzer format. The DMFT, at present, is capable of supplying 8 inputs to a chip and monitoring 8 outputs. Each input and output sequence may be as many as 4096 bits long.

Since a codeword for this RS code contains 255 symbols, the computation of a complete codeword requires 255 "symbol cycles." A symbol cycle is the time interval required for executing a complete cycle of Berlekamp's algorithm. Since a symbol consists of 8 bits, a symbol cycle contains 8 "bit cycles." A bit cycle is the time interval for executing one step in Berlekamp's algorithm.

In this design, a bit cycle corresponds to one period of the clock. The total number of clock cycles required to encode a single RS codeword is therefore 255 × 2040.

The chip was successfully tested at up to 3.2 MHz using the DMFT. At the maximum clock rate, the chip consumed 100 mW of power.

[1] See also M. Perlmen and J. J. Lee, "Reed-Solomon Encoders – Conventional Versus Berlekamp's Architecture," Interoffice Memo No. 3610-81-119 ISPM (internal document), Jet Propulsion Laboratory, Pasadena, CA.

[2] *Ibid.*, Figure 3.

[3] *Ibid.*; see Figure 6 for the original layout of the encoder.

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The authors wish to acknowledge M. Perlman and J. J. Lee who brought the Berlekamp algorithm to our attention and worked with Berlekamp to produce the prototype discrete IC encoder upon which this chip is modeled. Additionally, the authors wish to thank Erlend Olson who designed the DMFT system in response to our particular testing needs.

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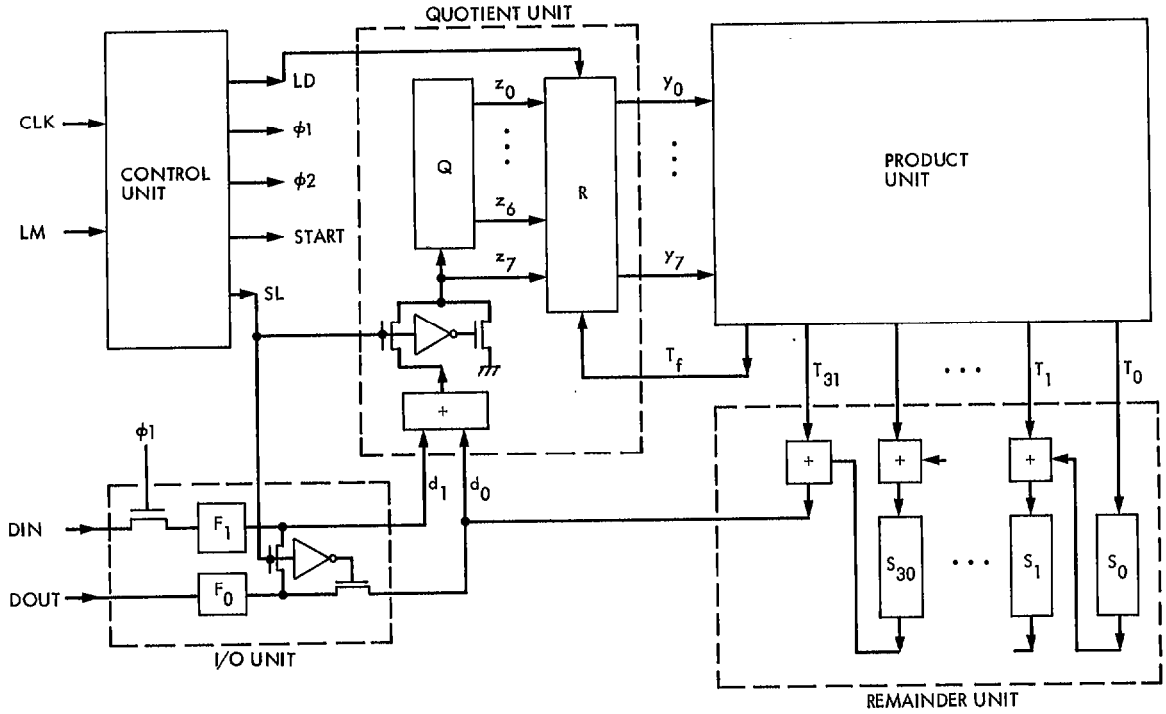

Fig. 1. Block Diagram of the (255, 223) RS encoder

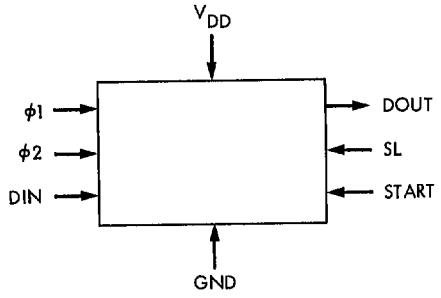

Fig. 2. The symbolic diagram of a (255, 223) RS encoder chip

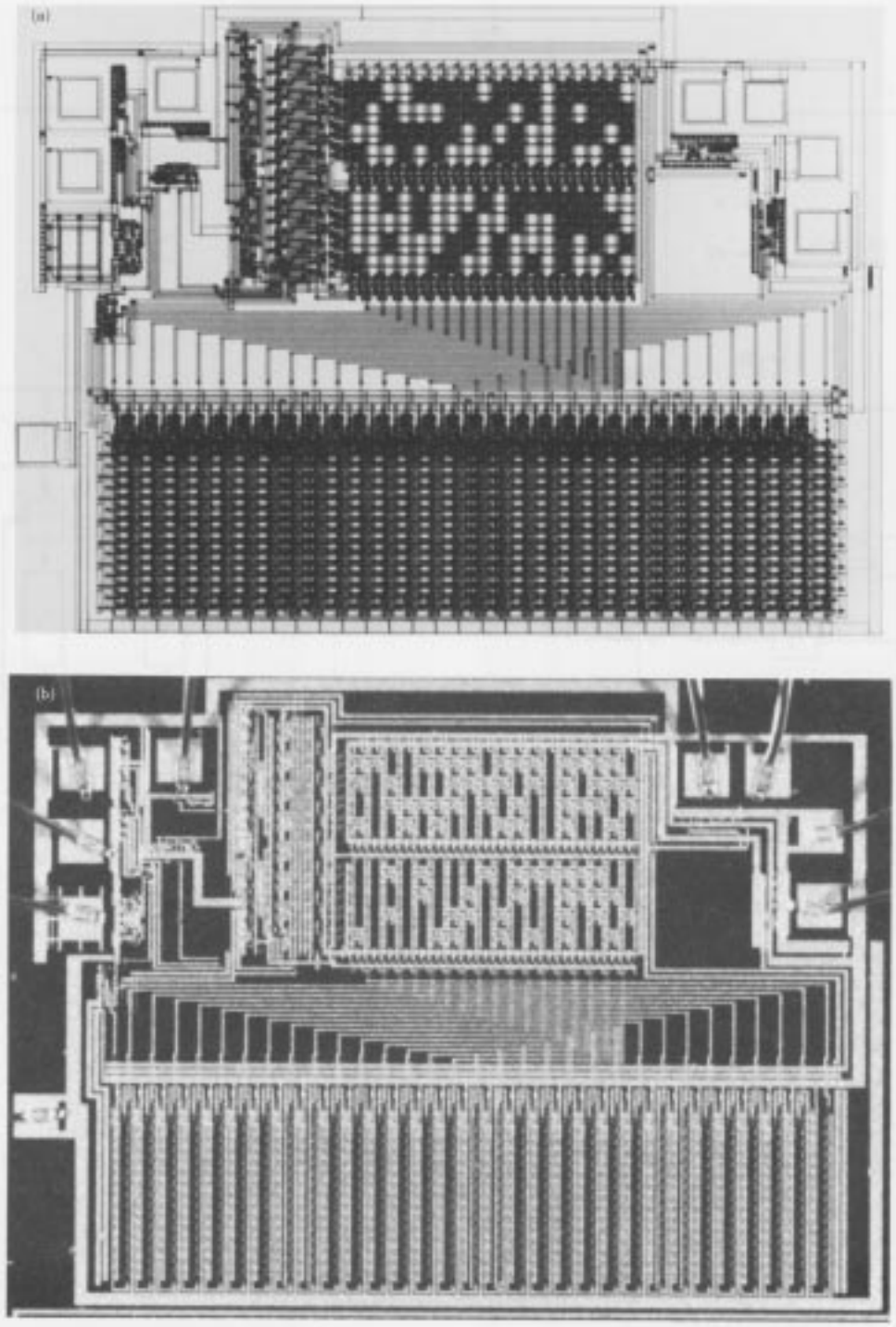

Fig. 3. The (255, 223) RS encoder chip: (a) layout, (b) photograph of working chip